



EV 317135668 #20/D
6/19/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee KMT Semiconductor, LTD and Micron Technology, Inc.
Group Art Unit
Examiner Quang D. Vu
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

RESPONSE TO APRIL 23, 2003 FINAL OFFICE ACTION
ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION (RCE)

To: Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: D. Brent Kenady
Tel. 509-624-4276; Fax 509-838-3424
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

RECEIVED
JUN 18 2003
TECHNOLOGY CENTER 2800

Responsive to the Final Office Action dated April 23, 2003, Applicant amends and remarks as follows:

AMENDMENTS

Underlines indicate insertions and ~~strikeouts~~ indicate deletions.